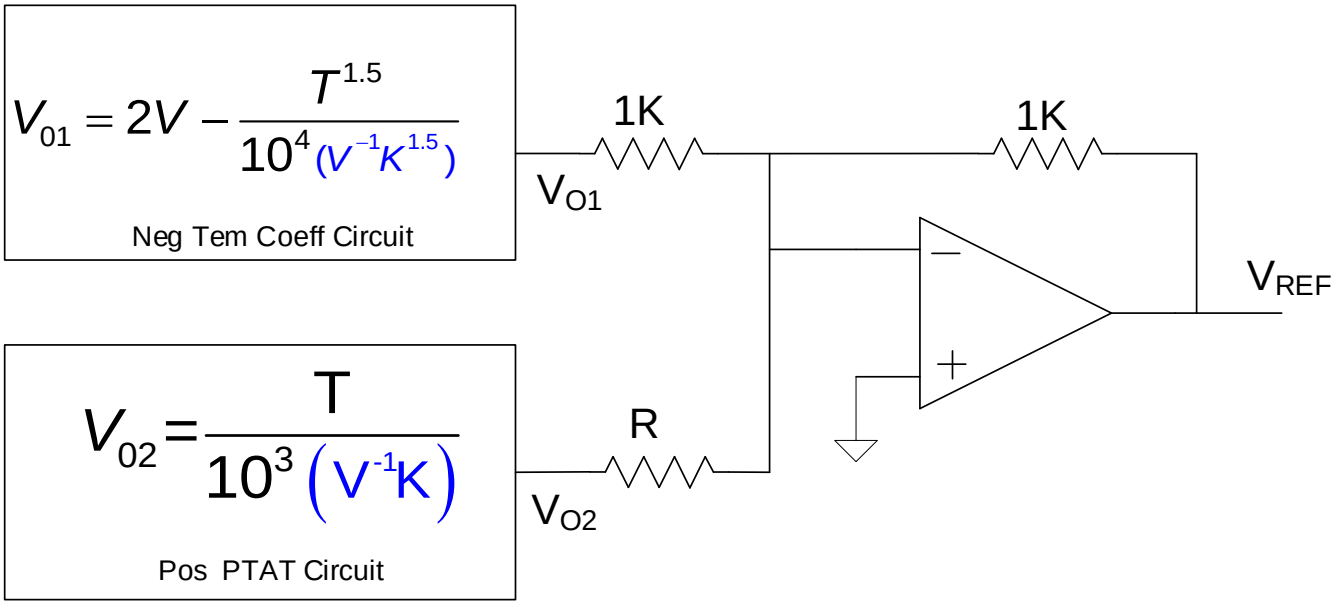
EE 435 Name_____
Final Exam
Spring 2020

Instructions: This is an open-book, open-notes exam. It is due at 12 noon on Thursday May 7. The solutions should be uploaded in a single .pdf file in Canvas. Please use black ink when solving the problems so that the scanned image is easy to read. All problems are equally weighted. On those problems that need technology parameters, assume you are working in a 0.5µm CMOS process with key parameters $\mu_n C_{OX}=100\mu A/v^2$, $\mu_p C_{OX}=30\mu A/v^2$, $V_{TNO}=0.8V$, $V_{TPO}= - 0.8V$, $C_{OX}=2fF/\mu^2$, $\lambda =0.01v^{-1}$, $\gamma = 0$, Cbdbot = $0.5fF/\mu^2$, and Cbdsw = $2.5fF/\mu$. All solutions should be provided on the exam sheet itself. If additional space is needed for solving a problem, use another unlined sheet of paper.

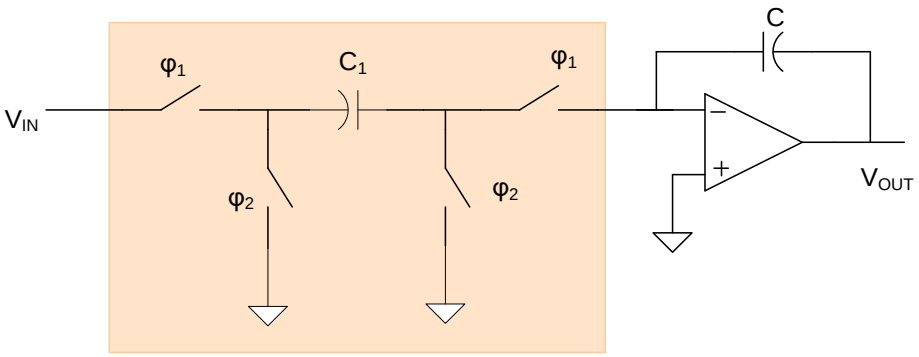
Problem 1 A 12-bit string DAC has an INL of 6 LSB. Determine the ENOB from an INL perspective.

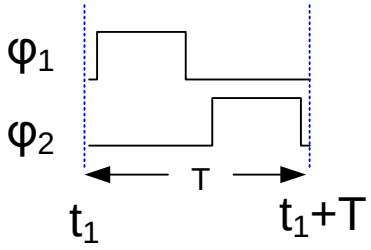
Problem 2 The circuit shown has been proposed as a voltage reference. It has two temperature sensors, one with a positive temperature coefficient and the other with a negative temperature coefficient. (The two boxes on the left are assumed to be voltage sources with zero output impedance and output voltages given by the equations shown in the figure.)

a) Determine R so that the temperature coefficient of V_{REF} is 0 at T=300K.
b) With the value of R determined in part a), what is the maximum deviation in V_{REF} from the value output at 300K for 250K<T<350K?



Problem 3 Assume that C=10pf, C_1=500fF, and the switches and op amp are ideal. The switched are clocked with a complimentary nonoverlapping clock. One period of the clock waveform is shown below where the clock period of 1usec. If V_{IN}=0.2sin(2000t), determine V_{OUT}(t). Assume the op amp is ideal.





Problem 4 Consider an ideal 10-bit ADC with a reference voltage of 2.5V. If a 1KHz triangle wave with a 0.5V p-p swing centered at 1.25V is presented to the input to the ADC, determine

a) The quantization noise of the ADC
b) The signal to noise ratio of the ADC output for the input signal specified

Problem 5 A periodic signal was applied to a DAC and the output was sampled 4096 times at 1msec spacings over precisely 11 periods of the output. A DFT using the FFT was used to obtain the DFT of the sampled sequence. The magnitude of the first 120 terms, expressed in DB, are given on the following page. All remaining terms were smaller than -95dB.

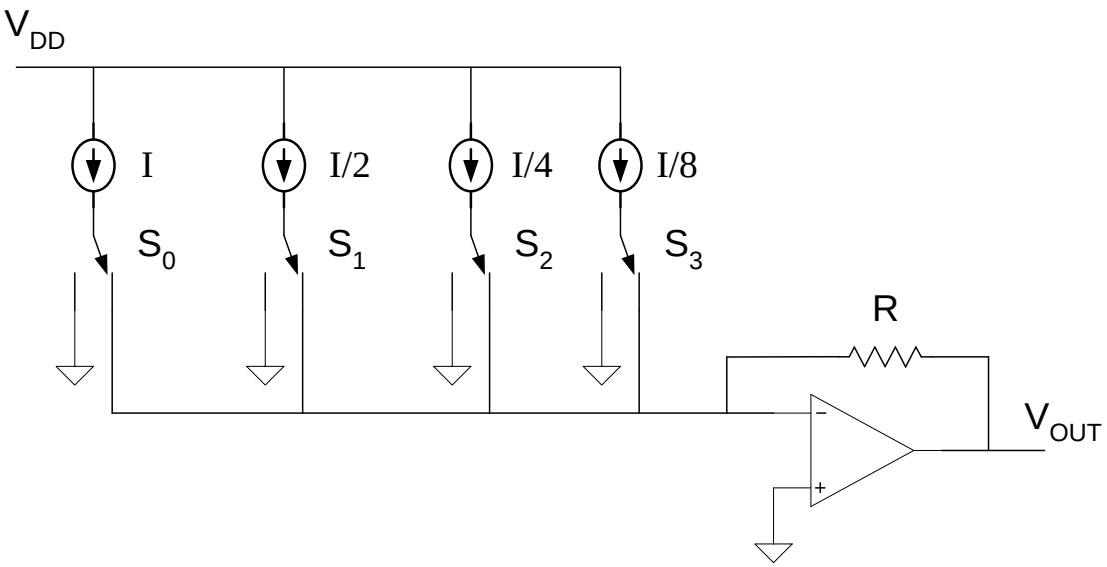
a) What is the magnitude of the signal?
b) What was the frequency of the signal?
c) What is the SFDR?
d) What is the THD?

Index Number	Mag (dB)	Index Number	Mag (dB)	Index Number	Mag (dB)
1	-97.23	41	-99.21	81	-99.21
2	-98.4	42	-97.43	82	-97.43
3	-96.3	43	-95.61	83	-95.61
4	-99.21	44	-97.4	84	-97.4
5	-97.43	45	-97.23	85	-97.23
6	-95.61	46	-98.2	86	-98.2
7	-97.4	47	-99.4	87	-99.4
8	-97.23	48	-98.78	88	-98.78
9	-98.2	49	-99.21	89	-97.23
10	-99.4	50	-97.43	90	-99.21
11	-98.78	51	-95.61	91	-97.43
12	2.001	52	-97.4	92	-95.61
13	-96.3	53	-97.23	93	-97.4
14	-99.21	54	-98.2	94	-97.23
15	-97.43	55	-99.4	95	-98.2
16	-95.61	56	-98.78	96	-99.4
17	-97.4	57	-97.23	97	-98.78
18	-97.23	58	-98.4	98	-97.23
19	-98.2	59	-96.3	99	-98.4
20	-99.4	60	-99.21	100	-96.3
21	-98.78	61	-97.43	101	-99.21
22	-97.23	62	-95.61	102	-97.43
23	-53.2	63	-97.4	103	-95.61
24	-96.3	64	-98.78	104	-97.4
25	-99.21	65	-98.83	105	-98.78
26	-97.43	66	-96.3	106	-98.3
27	-95.61	67	-99.21	107	-96.3
28	-97.4	68	-97.23	108	-99.21
29	-98.78	69	-98.4	109	-97.43
30	-98.3	70	-96.3	110	-95.61
31	-96.3	71	-99.21	111	-97.4
32	-99.21	72	-97.43	112	-97.23
33	-97.43	73	-95.61	113	-97.23
34	-67.9	74	-97.4	114	-98.4
35	-97.4	75	-98.78	115	-96.3
36	-97.23	76	-98.3	116	-99.21
37	-98.2	77	-96.3	117	-97.43
38	-99.4	78	-99.21	118	-95.61
39	-98.78	79	-97.43	119	-97.4
40	-97.23	80	-95.61	120	-98.78

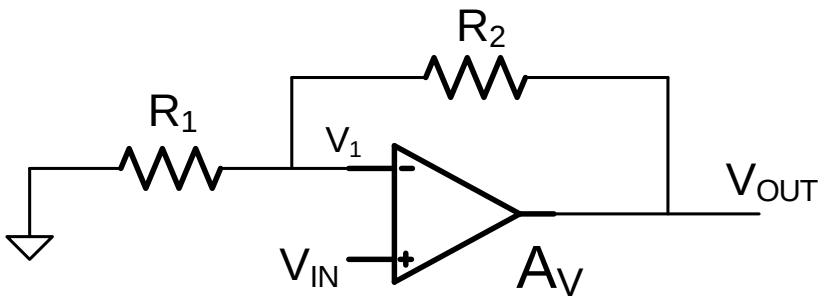
Problem 6 Consider the DAC circuit shown below.

a) Derive an expression for the output voltage as a function of the Boolean inputs S_0, S_1, S_2 and S_3..

b) If the current source above S_0 is 10% below the nominal value and all other current sources are equal to their nominal values, determine the INL of this DAC.



Problem 7 An op amp with an open-loop dc gain of 10^5 has two open-loop poles and no open-loop zeros. The ratio of the poles is $2x10^5$. If this op amp is used in the design of a basic noninverting feedback amplifier shown below, determine the closed loop pole Q and the phase margin of the feedback amplifier. Assume the output impedance of the op amp is 0.



Problem 8

Answer the following questions.

a) In a hybrid DAC architecture, the input is often partitioned into an MSB part and a LSB part. The MSB part of the input is often used as the input to a thermometer coded DAC and the LSB part of the input is often used as the input to a binary-coded DAC. What is the major reason this approach is often used?

b) In the bandgap circuits discussed in class, the ratio of the currents in the two diodes was kept constant independent of temperature. Why was this done?

c) What layout strategy is used to eliminate the effects of linear gradients in device parameters?

d) It was observed that a rapidly switched capacitor behaves as a resistor. Though this relationship was observed by Maxwell in the late 1800's, it was little more than an academic curiosity at the time. But in the late 1970's two important properties of circuits that used switched capacitors to implement resistors were recognized. What were those two important properties?

e) Miller compensation of an op amp was a major breakthrough but strict Miller compensation results in a zero on the positive real axis and this is undesireable. What simple circuit modification is often used to move the RHP zero to the negative real axis where performance of the circuit can actually be improved?

f) When compensating an op amp, dominant pole compensation is often used to move the pole on the output of the first stage to a very low frequency. Why is it not advantageous to also move the pole on the second stage to a lower frequency?

g) Switching currents on and off in a current-steering DAC causes large glitches on the output and long settling times to turn on and off the current sources. What strategy is used to dramatically reduce the glitches and settling time in current steering DACs?